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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,168	07/11/2003	Alan Kykcr	42P7938C	4367

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER
PEUGH, BRIAN R

ART UNIT	PAPER NUMBER
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rcv. 10/06)

	Application No.	Applicant(s)
Office Action Summary	10/618,168	KYKER ET AL.
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>17 October 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,12-15,18-20,22-28 and 30* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 12-15, 18-20, 22-28, and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some *   c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed October 17, 2006 in response to PTO Office Action dated September 27, 2006 The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-6, 12-15, 18-20, 22-28, and 30 have been presented for examination in this application. In response to the last Office Action, claims 1, 18, 19, and 27 have been amended.

Claim Objections

Claim 12 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim {newly amended claim 1]. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as

set forth in section 102 of this title, if the differences between the subject matter sought to be

patented and the prior art are such that the subject matter as a whole would have been obvious

at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains. Patentability shall not be negatived by the manner in which the invention

was made.

Claims 1-6, 12, 19, 20, 22-24, 27, 28, and 30 are rejected under 35

U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) or

Quattromani (US Patent No. 5,835,949) in view of Jensen (US Patent No. 5,133,058)

and Krick et al. (US Patent No. 6,018,786).

As per claim 1, 19, 23-24, and 27, AAPA discloses a memory controller to

coupled to a memory **[104]** and one or more microprocessors **[115; claim is not**

positively recited such that the coupling has actually occurred, rather that the

controller is available to be coupled]; an execution unit **[118]** coupled to the memory

controller, the execution unit to trigger a snoop if a store into the memory occurs **[page**

7, lines 4-9 & 19-20]; ...an instruction decoder ...an instruction cache 114 that is

physically addressed, wherein a snoop is triggered by storing into memory 104 **[page 7,**

lines 19-20], it performs self modifying by comparing the physical addresses stored

within the cache **[page 7, lines 20-24]**. AAPA further discloses that when a mach is

indicated, the instruction cache is flushed **[page 7, line 25 through page 8, line 1]**.

AAPA discloses the claimed invention, but fails to specifically teach a trace cache and that the comparison is within a ITLB having a content addressable memory.

Krick et al. teaches use of a trace cache **[col. 4, lines 22-34]**.

Jensen teaches a ITLB having a content addressable memory for performing snoop accesses of physical addresses and comparing the physical addresses in the TLB with the physical addresses snooped; the TLB stores page translation between linear addresses and physical pages **[translation look-aside buffer 32 having a portion 52 that may be constructed as a content addressable memory (column 8, lines 16-34); comparator is used to match the physical addresses sought with the physical addresses stored in the TLB (column 9, line 67 through column 10, line 3)]**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the current invention to modify AAPA such that the comparison of the physical addresses occurs in a TLB as being taught by Jensen in order to have a faster system by obviating the problem of time consuming page walks **[column 2, lines 12-43 and column 7, lines 11-12]**, as well as including a specific trace cache in order to facilitate a greater amount of instructions [col. 4, lines 22-34], as taught by Krick et al.

As for claim 2, AAPA discloses that if it is determined that the physical address received by the TLB matches a physical page address stored within the TLB, indicating that information was modified within the memory correlating to information potentially

located within the cache, information within the cache is invalidated **[page 7, line 25 through page 8, line 1]**.

As for claim 3, AAPA discloses that information within the cache is invalidated by setting a bit in the cache to indicate invalid information in a cache line and disregarding the information within the cache **[it is inherent in the art that when a cache line is flushed, the valid bit associated with that line would be set to invalid]**.

As for claims 4, 20 and 28, AAPA discloses that if it is determined that the physical address received by the TLB matches a physical page address stored within the TLB, indicating that information was modified within the memory correlating to information potentially located within the cache or a pipeline, and the microprocessor provides inclusion for the cache and the pipeline such that information within the cache and the pipeline are invalidated **[when an SMC match, the cache memory and instruction pipeline are flushed (page 7, line 25 through page 8, line 1)]**.

As for claim 5, AAPA discloses that information within the cache and a pipeline are invalidated by setting a bit in the cache to indicate invalid information in a cache line and disregarding the information within the cache and the pipeline **[it is inherent in the art that when a cache line is flushed, the valid bit associated with that line would be set to invalid; disregarding the instructions in the pipeline (page 5, lines 1-3)]**.

As for claim 6, AAPA discloses that the TLB maintains original page translations

for all bytes of information within the cache and pipeline to provide inclusion

instructions pipeline are guaranteed to stay in the instruction cache (page 7, lines

11-15)].

As for claims 12, 22, and 30 Jensen teaches that the cache is an instruction

cache and the TLB is an instruction TLB **[see Fig. 3]**.

Claims 13-15, 18, 23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Quattromani (US Patent No. 5,835,949) in view of Jensen (US Patent

No. 5,133,058).

As for claim 13, Quattromani discloses an instruction cache which, stores

translation between a linear addresses and physical addresses for the cache entries.

Quattromani further discloses comparison between the physical address of a write to

the physical address tags in the cache to determine if the data stored in the cache

memory **[cache 65 (Fig. 5); column 10, lines 14-23 and 39-41]**.

Jensen teaches a TLB having a content addressable memory for performing

snoop accesses of physical addresses and comparing the physical addresses in the

TLB with the physical addresses snooped; the TLB stores page translation between

linear addresses and physical pages **[translation look-aside buffer 32 having a**

portion 52 that may be constructed as a content addressable memory (column 8,

lines 16-34); comparator is used to match the physical addresses sought with the

physical addresses stored in the TLB (column 9, line 67 through column 10, line 3)].

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the current invention to modify Quattromani such that the comparison of the physical addresses occurs in a TLB having a content addressable memory instead the AAPA's instruction cache as being taught by Jensen in order to have a faster system by obviating the problem of time consuming page walks **[column 2, lines 12-43 and column 7, lines 11-12]**.

As for claim 14, Quattromani discloses that the comparing generates a match between the provided physical memory address and one or more of the physical page memory addresses included in the stored page table translations indicating the potential occurrence of self modifying code and cache incoherency **[column 10, lines 21-26 and 39-41]**.

As for claim 15, Quattromani teaches invalidating the instructions within the cache memory and an instruction pipeline for execution and fetching new instructions from the physically addressable memory to overwrite the invalidated instructions after the comparing generates a match indicating the potential occurrence of self modifying code and cache incoherency **[column 10, lines 21-26]**.

As for claim 18, Quattromani teaches maintaining original stored page table

translations for all bytes of information within the cache memory and an instruction

pipeline [column 2, lines 33-41].

As for claim 23, Quattromani discloses the limitation as set forth for the rejection

of claim 13 and in addition discloses that a hit to the physical address in the cache

results in invalidation of that entry.

Jensen teaches a TLB having a content addressable memory for performing

snoop accesses of physical addresses and comparing the physical addresses in the

TLB with the physical addresses snooped; the TLB stores page translation between

linear addresses and physical pages [translation look-aside buffer 32 having a

portion 52 that may be constructed as a content addressable memory (column 8,

lines 16-34); comparator is used to match the physical addresses sought with the

physical addresses stored in the TLB (column 9, line 67 through column 10, line

3)].

Therefore, it would have been obvious to one having ordinary skill in the art at

the time of the current invention to modify Quattromani such that the comparison of the

physical addresses occurs in a TLB having a content addressable memory instead the

AAPA's instruction cache as being taught by Jensen in order to have a faster system by

obviating the problem of time consuming page walks [column 2, lines 12-43 and

column 7, lines 11-12].

As for claim 25, Quattromani discloses invalidating the information stored into an instruction pipeline from the cache upon generation of the self-modifying code hit signal **[column 10, lines 21-26]**.

As for claim 26, Quattromani discloses fetching instructions from memory to rewrite the information into the cache to obtain cache coherency **[column 10, lines 35-39]**.

Response to Arguments

Applicant's arguments with respect to claims 1-6, 12, 19, 20, 22-24, 27, 28, and 30 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the 35 U.S.C. 103(a) rejection for claims 1-6, 12, 19, 20, 22-24, 27, 28, and 30, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Applicant states that "..significant modifications " would be required for the references to be combined with AAPA, however details regarding claim limitations in support of this statement have not been made.

Regarding the 35 U.S.C. 103(a) rejection for claims 13-15,18, 23, 25, and 26, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the

references. Applicant states that "..significant modifications " would be required for the references to be combined with AAPA, however details regarding claim limitations in support of this statement have not been made.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
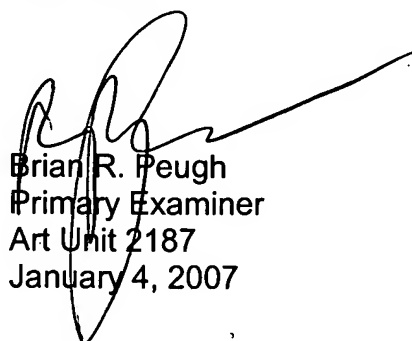
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Primary Examiner
Art Unit 2187
January 4, 2007